In the Claims:

Claims 1 to 33 stand of record in the case.

Claims 1, 3, 6 to 18 and 20 to 33 stand rejected.

Claims 2, 4, 5 and 19 are objected to.

Explanation of Amendments in the Claims:

1.(currently amended) Apparatus for directly generating a QAM RF signal comprising:

a high speed reference clock providing in an input signal having a series of pulses at a frequency of the reference clock which is higher than the desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses of the input reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors;

and a signal combining element for receiving the digital vectors from the programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated and in which the output frequency is determined by an increment value.

2.(currently amended) ~~The apparatus according to Claim 1~~ Apparatus for directly generating a QAM RF signal comprising:

a high speed reference clock providing in an input signal having a series of pulses at a frequency of the reference clock which is higher than the desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses of the input reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors;

and a signal combining element for receiving the digital vectors from the programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated;

wherein there are provided amplifiers for amplifying the digital vectors non linearly before combining.

3.(currently amended) The apparatus according to Claim 1 wherein the programmable digital delay elements comprise high speed adders/accumulators wherein said adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference signal.

4.(currently amended) ~~The apparatus according to Claim 3~~ Apparatus for directly generating a QAM RF signal comprising:

a high speed reference clock providing in an input signal having a series of pulses at a frequency of the reference clock which is higher than the desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses of the input reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors;

and a signal combining element for receiving the digital vectors from the programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated;

wherein the programmable digital delay elements comprise high

speed adders/accumulators wherein said adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference signal; and

wherein the ~~output frequency is set from an~~ increment value is set according to the following equation:

~~Increment Value = $((f_{ref} / f_{out}) -1) * 2^n$~~

Increment Value = $((f_{ref} / f_{out}) -1) * 2^n$

where f_{ref} = Reference clock (103) frequency

f_{out} = Output (110) frequency

n = Number of bits in the accumulator math.

5.(currently amended) ~~The apparatus according to Claim 3~~ Apparatus for directly generating a QAM RF signal comprising:

a high speed reference clock providing in an input signal having a series of pulses at a frequency of the reference clock which is higher than the desired output frequency;

two digitally controlled programmable digital delay elements each arranged to receive the reference pulses of the input reference clock and to generate therefrom using input data a respective one of two fixed amplitude output digital vectors;

and a signal combining element for receiving the digital vectors from the programmable digital delay elements and for generating the QAM RF signal therefrom which signal is amplitude and phase modulated;

wherein the programmable digital delay elements comprise high

speed adders/accumulators wherein said adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference signal; and

wherein the duty cycle of the digital vectors is set by initializing the difference of the initializing values of the two accumulators according to the following equation:

The reference clock frequency divided by the desired output frequency multiplied by $\underline{2^n}$ $\cancel{2^n}$ multiplied by (p/100), where p is the percentage duty cycle and n is the number of bits in the accumulator math.

6.(original) The apparatus according to Claim 1 wherein said reference clock is an external input with high frequency absolute accuracy and very low phase noise performance.

7.(original) The apparatus according to Claim 1 wherein said delay elements delay a reference edge of the input reference clock.

8.(currently amended) The apparatus according to Claim 7 wherein said reference edge of the input reference clock may be either the rising or falling edge of the reference clock.

9.(original) The apparatus according to Claim 1 wherein said delay elements have separate controls for producing the rising and falling edges of the output from the same input edge of the reference clock.

10.(original) The apparatus according to Claim 1 wherein implementation of the delay elements may vary by altering the input clock signal.

11.(original) The apparatus according to Claim 3 wherein said

adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference edge to produce the desired RF frequency.

12.(original) The apparatus according to Claim 1 wherein said programmable digital delay elements include modulation adders which add in the positive or negative phase offset to the accumulator value to produce the required modulation.

13.(original) The apparatus according to Claim 1 wherein there is provided an interpolator which interpolates the input data in the form of base band modulated information.

14.(currently amended) The apparatus according to Claim 13 wherein the interpolator is a linear interpolator or a (sin x)/x ~~sin x/x~~ interpolator filter.

15.(original) The apparatus according to Claim 13 wherein the interpolator effects interpolation up to the reference clock rate so as to avoid use of a reconstruction filter.

16.(currently amended) The apparatus according to Claim 1 wherein ~~an~~ there are provided separate interpolators for both the rising and falling pulse edges.

17.(original) The apparatus according to Claim 1 wherein there is provided a pulse swallow circuit which is arranged to ignore/block multiple reference clock pulses.

18.(original) The apparatus according to Claim 17 wherein the

pulse swallow circuit is arranged such that it controlled by the carry bits (overflow bits) in order to extend the delay to multi cycles of the input reference clock.

19.(original) The apparatus according to Claim 17 wherein said pulse swallow circuit is located prior to or following the programmable delay element.

20.(currently amended) The apparatus according to Claim 1 wherein the programmable digital delay elements are arranged such that 360 degrees of phase delay of the programmable delay is calibrated to $\underline{2^n}$ ~~2^n~~ of the phase accumulator value using a look up table or microprocessor.

21.(original) The apparatus according to Claim 20 wherein the lookup table has a multiple set of lookup tables to be used for temperature compensation of the programmable delay element.

22.(original) The apparatus according to Claim 1 wherein said signal combining element comprises flipflops which are used to combine the separate rising and falling edge delays to form any desired duty cycle output.

23.(original) The apparatus according to Claim 22 wherein the programmable digital delay elements are arranged such that said duty cycle of the output is varied by changing the difference in the initialization values of the accumulators for the rising and falling edge delay control.

24.(original) The apparatus according to Claim 22 wherein the programmable digital delay elements are arranged such that said output duty cycle is not dependent on the input duty cycle.

25.(original) The apparatus according to Claim 22 wherein the two

phase modulated vector outputs of the flipflops is amplified using nonlinear amplifiers.

26.(original) The apparatus according to Claim 8 wherein said increment values for the rising and falling edges are the same value.

27.(currently amended) The apparatus according to Claim 3 wherein the programmable digital delay elements are arranged such that the worst case frequency resolution is determined by the equation: The reference frequency divided by 2^n ~~2^n~~, where n is equal to the number of bits in the accumulator.

28.(original) The apparatus according to Claim 3 wherein the programmable digital delay elements are arranged such that increasing the number of bits in the adder math increases the frequency resolution with negligible degradation in the phase noise performance.

29.(original) The apparatus according to Claim 3 wherein the programmable digital delay elements are arranged such that the number of bits of math used in the adder can be equal to or exceed the number of bits of control in lookup table and /or the programmable delay.

30.(original) The apparatus according to Claim 3 wherein the programmable digital delay elements include parallel processing in the adders and/or accumulators to increase the speed.

31.(currently amended) The apparatus according to Claim 3 wherein the programmable digital delay elements are arranged such that the adders/accumulators are ~~can be~~ implemented in a ~~larger~~ lookup table containing

data which is ~~wherein all the answers of the pattern are~~ precomputed and stored.

32.(original) The apparatus according to Claim 1 wherein the components are formed fully digitally in an ASIC with no requirement for a voltage controlled oscillator, loop filter, or Digital to Analog converter.

33.(original) The apparatus according to Claim 1 wherein there is further provided amplification and filtering of the output to produce a signal that is higher in amplitude and/or having less harmonics.